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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,867	01/20/2004	YAO-CHI WANG	11870-US-PA	1866

31561 7590 11/04/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 11/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,867	WANG, YAO-CHI	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on 9/02/05.

Response to Brief

2. Applicant's argument "storing a portion of charges of the input signal " of the claimed invention have been considered and overcome Kusumoto and Zhou. The Final rejection from previous office action is withdrawn, and new ground of rejection is applying to this office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 4, 7 – 9, 10 – 13, and 16 - 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Aram et al. U.S. Patent No. 6,400,241.

Regarding claim 1, Fig. Fig. 4A – 4C discloses a threshold voltage control circuit, comprising: a first capacitor (CP2), having a first terminal and a second terminal (top and bottom terminals of capacitor CP2), wherein said first terminal (bottom terminal of capacitor CP2) is coupled to a first voltage level (Ground); a clock generator (Fig. 3[20]; also see Fig. 5) for generating a plurality of clock signals (**Φ1, Φ2, ΦA, ΦB**) and a switching capacitor network (CP1), coupled to

said second terminal of said first capacitor (Top terminal of capacitor CP2), wherein the switching capacitor network (CP1) receives an analog signal (Vrefp) and said clock signals (**Φ1, Φ2, ΦA, ΦB**), stores a portion of charges of said analog signal (See VCP1 and **ΦA** of Fig. 5), and outputs said portion of charges according to said clock signals (**ΦA**), and generates a threshold voltage associated with said first capacitor (Col. 5 lines 9 - 29).

Regarding claim 2, wherein said switching capacitor network comprises a plurality of sensor control switches (switches at **Φ1, Φ2, ΦA, ΦB**), wherein one of controlled by said clock said sensor control switches is signals for turning on/off (Fig. 4A – 4C), said sensor control switches (**Φ1, Φ2, ΦA, ΦB**) are series-connected to for a series structure (Fig. 4A – 4C) having a first terminal and a second terminal (left and right terminals of switches), said first terminal of said series structure receiving said analog signal (Vrefp) and said second terminal of series structure being coupled to said second terminal of said first capacitor (top terminal of CP2) to output said threshold voltage (Vo), and at least a second capacitor (CP1), having a first terminal (top terminal of CP1) and a second terminal (bottom terminal of CP1), wherein said first terminal of said second capacitor (top terminal of CP1) is coupled to a node connected to two adjacent sensor control switches (node between **ΦA and ΦB**) in said series structure, said second terminal of said second capacitor is coupled to a second voltage level (Ground Level).

Regarding claim 3, wherein said of clock signals (**Φ1, Φ2**) have a same frequency with different phases respectively (Fig. 5).

Regarding claim 4, wherein said pluralities of clock signals do not overlap (**Φ1 does not overlap Φ2; and ΦA does not overlap ΦB**).

Regarding claim 7, wherein said circuit applies to a frequency-shift keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

Regarding claim 8, wherein said circuit applies to an amplitude-shift keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

Regarding claim 9, wherein said circuit applies to an on/off keying communication system (this claim is intend of use only, since it has been held that a recitation with respect to the manner in which claim apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. *Ex parte Masham,* 2 USPQ2d 1647 (1987)).

Regarding claim 10, Fig. 3 of Aram et al. discloses an analog-to-digital converter (10), comprising: a first capacitor (Fig. 4A is a detailed circuit of 101 in Fig. 3), Fig. 4A – 4C having a first terminal and a second terminal (top and

bottom terminals of capacitor CP2), wherein said first terminal (bottom terminal of capacitor CP2) is coupled to a first voltage level (Ground); a clock generator (Fig. 3[20]; also see Fig. 5) for generating a plurality of clock signals (**Φ1, Φ2, ΦA, ΦB**) and a switching capacitor network (CP1), coupled to said second terminal of said first capacitor (Top terminal of capacitor CP2), wherein the switching capacitor network (CP1) receives an analog signal (Vref through 134, 132, **Φ1, Φ2, ΦA**) and said clock signals (**ΦA, Φ2**) stores a portion of charges of said analog signal (Vrefp feedback is a portion of analog signal Vref), and outputs said portion of charges according to said clock signals (See VCP1 and **ΦA** of Fig. 5), and generates a threshold voltage (Vo) associated with said first capacitor (Col. 5 lines 9 - 29); and a comparator (134), for comparing (134) said threshold voltage (Vo) with analog signal (Vref) and outputting a digital signal (16).

Regarding claims 11 – 13, and 16 – 18, the claims incorporated the same subject matter as of claims 2 – 4 and 7 – 9 respectively, and rejected along the same rationale.

Regarding claim 19, Fig. 4A – 4C of Aram et al. discloses a method for converter an analog signal to a digital signal (Col. 2 lines 30 - 32), comprising: providing a first capacitor (CP2) and a plurality of clock signals (**Φ1, Φ2, ΦA, ΦB**); storing (CP1) a portion of charges of an analog signal (Vref) according to said clock signals (**Φ1, Φ2, ΦA, ΦB**), generating a threshold voltage (Vo) according to said clock signals (Col. 8 lines 13 - 21) based on said portion of charges associated with said first capacitor (VCP2); and comparing (134) said

threshold voltage with said analog signal (Vref) in order to output a digital signal (16).

Regarding claim 20, Fig. 5 of Aram et al. further discloses wherein said clock signals comprises a first clock signal (Φ_A) and a second clock signal (Φ_B) said first and second clock signals have a same frequency but not overlapping , and said step of generating said threshold voltage further comprising: providing a second capacitor (CP1), conducting said analog signal (Vrefp) to said second capacitor (CP1) according to said first clock signal (Φ_A) to store said portion of charges (Col.5 lines 18 – 29) of said analog signal in said second capacitor (CP2), and conducting said first capacitor (CP2) and said second capacitor (CP1) in response to said second clock signal (Φ_B) in order to generate said threshold voltage (Vo) based on said portion of charges (VCP1) of said analog signal (Vrefp) associated with said first capacitor (CP2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 6, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aram et al. as applied to claim as applied to claim 4 above, and further in view of Hua U.S. Patent No. 6,864,919.

Regarding claim 5, Fig. 24 of Aram et al. as applied to claim 4 above, does not explicitly discloses wherein the plurality of sensor control switches (Switches at **Φ1, Φ2, ΦA, ΦB**) are MOSFETS.

Fig. 1 of Hua teaches an analog to digital converter having sensor control switches (102, 106) are MOSFETS for charge couple device capacitors.

Aram et al. and Hua are common subject matter for sensor switches for analog-to-digital. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the MOSFET switches taught by Hua et al. into the switches of Aram et al. because CMOS is a less expensive technology employing fewer mask layers and is more mature fabrication technology with greater commercial volume (Hua; Col. 1 lines 48 – 52).

Regarding claim 6, modified Aram et al. as applied to claim 5 above, further discloses wherein said first voltage level and said second voltage level are DC voltage levels (Ground).

Regarding claim 14 and 15, the claims incorporated the same subject matter as of claims 5 and 6 respectively above, and rejected along the same rationale.

Cited Reference

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references relate to switches capacitor for Analog to Digital converter.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

10/28/05

Linh Van Nguyen

Art Unit 2819